

OUTPUT BUFFER CIRCUIT

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- Europeans: H03K19/00P4

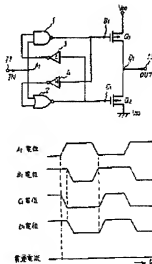
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Abstract of JP2114718

PURPOSE: To prevent malfunction of a circuit and to reduce current consumption by staggering the rise and fall times of gate inputs of a p-channel MOS transistor (TR) and an n-channel MOS TR so as to prevent overlapping and thereby preventing a through-current from flowing to the output. **CONSTITUTION:** When a potential at an input terminal 11, that is, at a point A1 rises from a low level to a high level, a potential at an output point C1 of a NOR gate 2 is descended. When an output of a low trip inverter 3 descended, the potential at an output of a NAND gate 1, that is, the potential of a point B1 is descended. Thus, the potential of the point B1 is being descended after the potential at the point C1 is sufficiently descended. An n-channel MOS TR Q2 is turned off at the trailing of the point C1 and a p-channel TR Q1 is first turned on at the rise of the point B1. Then a through-current flowing through the TRs Q1, Q2 is almost interrupted.



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